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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the so-called drive circuit one apparatus liquid crystal display which it really comes to form on the substrate with which poly-Si TFT (thin film transistor; thin film transistor) was arranged in the shape of a matrix about the liquid crystal display (LCD;Liquid Crystal Display) which carried a digital-to-analog circuit and this as a switching element whose drive circuit which includes the digital-to-analog circuit and this digital-to-analog circuit of a reference voltage selection mold especially is each pixel.
[0002]
[Description of the Prior Art] The conventional example of the drive circuit one apparatus liquid crystal display which really comes to form a digital interface drive circuit by TFT on the same substrate as a picture element part is shown in drawing 34 . In this drawing, the pixel has the composition which the 1st and 2nd level drive system 702,703 was allotted up and down, and the vertical-drive system 704 was allotted to the left-hand side of drawing, and was really formed on the same substrate (the LCD panel is called hereafter) with the effective pixel field 701 by TFT to the effective pixel field 701 which it comes to arrange in the shape of a matrix.
[0003] The 1st level drive system 702 is constituted by the level shift register 721, the sampling & 1st latch circuit 722, the 2nd latch circuit 723, and the DA (digital analog) conversion circuit 724. It is constituted by the level shift register 731, the sampling & 1st latch circuit 732, the 2nd latch circuit 733, and the DA translation circuit 734 like [the 2nd level drive system 703] the 1st level drive system 702. The vertical-drive system 74 is constituted by the perpendicular shift register 741.
[0004]
[Problem(s) to be Solved by the Invention] When the drive circuit one apparatus liquid crystal display of the above-mentioned configuration is created here, the magnitude of the field (this is hereafter called a frame) of the periphery of the field area 701 which really forms a drive circuit on the LCD panel, i.e., an effective pixel field, poses a big problem. Especially the circuit area of the DA translation circuit 724,734 serves as the important point at the time of deciding the magnitude of the frame of the LCD panel. As a DA translation circuit of a drive circuit one apparatus liquid crystal display, a reference voltage selection mold is used widely. The reason is because dispersion in output potential is small.
[0005] An example of the circuitry of a reference voltage selection mold DA translation circuit is shown in drawing 35 . This example of a circuit shows the case of the DA translation circuitry of triplet 8 gradation. This DA translation circuit has the composition of having formed the gradation selection unit 708-0 to 708-7 which consists of a selecting switch 705, a latch circuit 706, and a decoding circuit 707 in each gradation (reference voltages Vref0-Vref7) of every so that clearly from drawing 35 .
[0006] however, in the reference voltage selection mold DA translation circuit of this configuration Since the latch circuit 706 and the decoding circuit 707 are formed for every gradation and the element number which constitutes a circuit increases very much so that clearly from the circuitry of drawing 35 , When it is really going to form a multi-tone DA translation circuit by TFT, a very big circuit area is needed and the technical problem that the frame of the LCD panel becomes large and it becomes the hindrance of a miniaturization of the whole device in case it carries in a liquid crystal

display occurs as a result.

[0007] On the other hand, in order to attain contraction-ization of circuit area, taking the circuitry which combined the switched capacitor with the reference voltage selection mold DA translation circuit is also considered. However, in the case of this circuitry, since a buffer circuit is needed, only a part to consume in a buffer circuit has the technical problem that increase of system-wide power consumption is caused.

[0008] It is in offering the liquid crystal display which carried the DA translation circuit and this which can contribute to narrow-width-ization of the frame of the LCD panel, without making this invention in view of the above-mentioned technical problem, the place made into the purpose having few element numbers which constitute a circuit, ending, and moreover increasing power consumption.

[0009]

[Means for Solving the Problem] n polar analog switches corresponding to the logic of each bit of a n bits (n is two or more integers) data signal are mutually connected to a serial, and it becomes, and the DA translation circuit by this invention is 2n. 2n connected between each of the reference voltage line of a book, and an output line, respectively It has the composition of having the gradation selection unit of an individual. And this reference voltage selection mold DA translation circuit is carried as a DA translation circuit which constitutes a part of that drive circuit in a drive circuit one apparatus liquid crystal display.

[0010] In the liquid crystal display which carried the DA translation circuit of the above-mentioned configuration, and this, formation of the gradation selection unit of a configuration of that n polar analog switches corresponding to the logic of each bit of a data signal were mutually connected to the serial is attained with the same transistor in the decoding circuit which decodes a data signal, and the selecting switch which chooses the reference voltage to which it corresponds based on the decoding output by connect between a reference voltage line and the column line of a picture element part. Therefore, only the part will have few element numbers which constitute a circuit, and will end.

[0011]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail with reference to a drawing. Drawing 1 is the block diagram showing the system configuration of the drive circuit one apparatus liquid crystal display concerning 1 operation gestalt of this invention. In drawing 1 , to the effective pixel field 11 where it comes to arrange a pixel in the shape of a matrix, the 1st and 2nd level drive system 12 and 13 is allotted to the upper and lower sides, and the vertical-drive system 14 is allotted to the left-hand side of drawing.

[0012] In addition, it is not necessary to necessarily arrange the effective pixel field 11 up and down about a level drive system, and you may be up-and-down arrangement of only one side. Moreover, about a vertical-drive system, it may be arrangement on the right-hand side of drawing, or you may be arrangement of right-and-left both sides. And the 1st and 2nd level drive systems 12 and 13 and vertical-drive system 14 are really formed on the same substrate (the 1st substrate) as the effective pixel field 11 by TFT (thin film transistor). Opposite arrangement of the 2nd substrate (not shown) is carried out with predetermined spacing to this substrate. And the liquid crystal layer is held among both substrates.

[0013] The 1st level drive system 12 is constituted by the level shift register 121, the sampling & 1st latch circuit 122, the 2nd latch circuit 123, the level shifter 124, and the DA translation circuit (DAC) 125. It is constituted by the level shift register 131, the sampling & 1st latch circuit 132, the 2nd latch circuit 133, the level shifter 134, and the DA translation circuit 135 like [the 2nd level drive system 13] the 1st level drive system 12. The vertical-drive system 14 is constituted by the perpendicular shift register 141.

[0014] An example of the configuration of each pixel 20 in the effective pixel field 11 is shown in drawing 2 . The pixel 20 consists of TFT21 which is a switching element, a liquid crystal cell 22 by which the pixel electrode was connected to this drain electrode of TFT21, and auxiliary capacity 23 by which one electrode was connected to the drain electrode of TFT21. TFT21 of each pixel 20 is connected to low (line) line -- that gate electrode of whose is a perpendicular selection line, column (train) line [that source electrode of whose it connects with 24m-1, 24m, 24m+1, and --, and is a

signal line]--, 25n-1, 25n, 25n+1, and -- in this pixel structure.
[0015] Moreover, the counterelectrode of a liquid crystal cell 22 is connected to the common line 26 by which the common electrical potential difference VCOM is given. Here, the so-called common reversal driving method which reverses for example, the common electrical potential difference VCOM to every 1H (1 level period) is taken as a method of driving a liquid crystal cell 22. Since the polarity of the common electrical potential difference VCOM is reversed to every 1H by using this common reversal driving method, low-battery-ization of the 1st and 2nd level drive system 12 and 13 can be attained, and the power consumption of the whole device can be reduced.
[0016] Next, actuation of each part of the 1st and 2nd level drive system 12 and 13 is explained. In addition, although the following explanation takes and explains the 1st level drive system 12 to an example, the same thing can completely be said also about the 2nd level drive system 13.
[0017] In the 1st level drive system 12, the level transfer pulse [1] 1 HST, i.e., a level start pulse, and the level clock pulse HCK1 are given to the level shift register 121. Then, the level shift register 121 answers the level start pulse HST 1, and performs a horizontal scanning with the period of the level clock pulse HCK1. Synchronizing with the horizontal scanning of the level shift register 121, the sampling & 1st latch circuit 122 carries out the sequential sampling of the digital data, and latches the data sampled further to every column line --, 25n-1, 25n, 25n+1, and --.
[0018] The 2nd latch circuit 123 answers the latch signal which can be given 1H period, and re-latches the latch data corresponding to the column line latched by the sampling & 1st latch circuit 122 to every 1H. About the latch data re-latched by the 2nd latch circuit 123, a level shifter 124 carries out the level shift of the signal level (amplitude) to predetermined level, and supplies it to the DA translation circuit 125. In addition, about the level shifted in this level shifter 124, it mentions later.
[0019] On the other hand, in the vertical-drive system 14, the perpendicular transfer pulse VST, i.e., a perpendicular start pulse, and the perpendicular clock pulse VCK are given to the perpendicular shift register 141. Then, the perpendicular shift register 141 is answering the perpendicular start pulse VST and performing a vertical scanning with the period of the perpendicular clock pulse VCK, and gives a line selection signal one by one per line to the effective pixel field 11.
[0020] In addition, the reference voltage selection mold DA translation circuit outputted to the column line which chooses the target reference voltage and corresponds from the reference voltage for several gradation minutes in response to the data by which the level shift was carried out by the level shifter 124,134 as a DA translation circuit 125,135 of the 1st and 2nd level drive system 12 and 13 is used. The concrete circuitry of this reference voltage selection mold DA translation circuit 125,135 is the part by which it is characterized [of this invention].
[0021] The basic configuration of a reference voltage selection mold DA translation circuit is shown in drawing 3 . In addition, here shall take and explain the case where it is circuitry for which the reference voltages Vref0-Vref7 of 8 (= 23) gradation are prepared to an example to the digital data of a triplet (b2, b1, b0). Moreover, in drawing 3 , although the circuitry of the DA translation circuit corresponding to 25n of a certain column lines is shown, the DA translation circuit concerned is prepared for every column line.
[0022] In drawing 3 , eight gradation selection units 30-37 are formed to the reference voltages Vref0-Vref7 of 8 gradation. These gradation selection units 30-37 have the composition that three polar (straight polarity/negative polarity) analog switches corresponding to the logic of each bit (b2, b1, b0) of digital data were mutually connected to the serial. Namely, [0023] The gradation selection unit 30 has the composition that connected between the reference voltage line 38-0 of Vref0, and 25n of column lines, and the analog switch 301,302,303 of three negative polarity was mutually connected to the serial to data "000." The gradation selection unit 31 has the composition that connected between the reference voltage line 38-1 of Vref1, and 25n of column lines, and the analog switch 311,312 of two negative polarity and the analog switch 313 of the straight polarity of one piece were mutually connected to the serial to data "001."
[0024] The gradation selection unit 32 has the composition that connected between the reference voltage line 38-2 of Vref2, and 25n of column lines, and the analog switch 321 of negative polarity, the analog switch 322 of straight polarity, and the analog switch 323 of negative polarity were mutually connected to the serial to data "010." The gradation selection unit 33 has the composition

that connected between the reference voltage line 38-3 of Vref3, and 25n of column lines, and the analog switch 331 of one negative polarity and the analog switch 332,333 of the straight polarity of two pieces were mutually connected to the serial to data "011."

[0025] The gradation selection unit 34 has the composition that connected between the reference voltage line 38-4 of Vref4, and 25n of column lines, and the analog switch 341 of the straight polarity of one piece and the analog switch 342,343 of two negative polarity were mutually connected to the serial to data "100." The gradation selection unit 35 has the composition that connected between the reference voltage line 38-5 of Vref5, and 25n of column lines, and the analog switch 351 of straight polarity, the analog switch 352 of negative polarity, and the analog switch 353 of straight polarity were mutually connected to the serial to data "101."

[0026] The gradation selection unit 36 has the composition that connected between the reference voltage line 38-6 of Vref6, and 25n of column lines, and the analog switch 361,362 of the straight polarity of two pieces and the analog switch 363 of one negative polarity were mutually connected to the serial to data "110." The gradation selection unit 37 has the composition that connected between the reference voltage line 38-7 of Vref7, and 25n of column lines, and the analog switch 371,372,373 of the straight polarity of three pieces was mutually connected to the serial to data "111."

[0027] Drawing 4 is the circuit diagram showing an example of concrete circuitry which realizes the reference voltage selection mold DA translation circuit 125 of the basic configuration shown in drawing 3 , gives the same sign to drawing 3 and an equivalent part, and is shown. As three analog switches each of the gradation selection units 30-37 for 8 gradation, it has composition using the MOS transistor of the conductivity type (an N channel/P channel) corresponding to the logic of each bit (b2, b1, b0) of digital data.

[0028] In drawing 4 , the gradation selection unit 30 has composition corresponding to data "000" which has arranged these in series and was created, using both the MOS (it being hereafter described as PMOS) transistors Qp301, Qp302, and Qp303 of a P channel as an analog switch 301,302,303. The gradation selection unit 31 has composition which has arranged these in series and was created, using the PMOS transistors Qp311 and Qp312 corresponding to data "001", and the MOS (it being hereafter described as NMOS) transistor Qn313 of an N channel as an analog switch 311,312,313.

[0029] The gradation selection unit 32 has composition which has arranged these in series and was created, using the PMOS transistor Qp321 corresponding to data "010", the NMOS transistor Qn322, and the PMOS transistor Qp323 as an analog switch 321,322,323. The gradation selection unit 33 has composition which has arranged these in series and was created, using the PMOS transistor Qp331 and the NMOS transistors Qn332 and Qn333 corresponding to data "011" as an analog switch 331,332,333.

[0030] The gradation selection unit 34 has composition which has arranged these in series and was created, using the NMOS transistor Qn341 and the PMOS transistors Qp342 and Qp343 corresponding to data "100" as an analog switch 341,342,343. The gradation selection unit 35 has composition which has arranged these in series and was created, using the NMOS transistor Qn351 corresponding to data "101", the PMOS transistor Qp352, and the NMOS transistor Qn353 as an analog switch 351,352,353.

[0031] The gradation selection unit 36 has composition which has arranged these in series and was created, using the NMOS transistors Qn361 and Qn362 and the PMOS transistor Qp363 corresponding to data "110" as an analog switch 361,362,363. The gradation selection unit 37 has composition corresponding to data "111" which has arranged these in series and was created, using both the NMOS transistors Qn371, Qn372, and Qn373 as an analog switch 371,372,373.

[0032] In the reference voltage selection mold DA translation circuit 125 of the above-mentioned configuration Each of n polar analog switches corresponding to the logic of each bit of n bits (n>=2) digital data It creates using one PMOS transistor or one NMOS transistor. In the combination of a PMOS transistor and an NMOS transistor 2n corresponding to the target gradation Since the gradation selection unit of an individual is constituted, a DA translation circuit multi-tone in small area can be realized, and the LCD panel of a very narrow-width frame can be realized as a result. This is based on the following reasons.

[0033] ** It is for there being very few element numbers from which they constitute a circuit since the selecting switch 705 and the decoding circuit 707 in a circuit are formed with the same transistor,

and ending conventionally which is shown in drawing 35 .
** Since it approaches and the continuation formation of the PMOS transistor and NMOS transistor which the well for isolation does not exist in a TFT circuit, and serve as a switch can be carried out, it is for the occupancy area of a circuit to be very small and to end.
[0034] Reason for the above ** is further explained in full detail as compared with the structure of a single crystal silicon transistor. Here, the case where one NMOS transistor and one PMOS transistor are arranged and formed in series shall be taken and considered for an example.
[0035] First, considering the structure of a single crystal silicon transistor, as shown in drawing 5 , it has fixed spacing in the substrate front-face side of the P type silicon substrate 41, and it is N+. The diffusion fields 42 and 43 are formed and they are these N+. An NMOS transistor is formed above the channel between the diffusion field 42 and 43 by the gate electrode 45 being arranged through gate dielectric film 44. Here, it is N+. The diffusion field 42 turns into a drain / source field, and it is N+. The diffusion field 43 turns into the source / drain field.
[0036] On the other hand, in order to adjoin an NMOS transistor and to form a PMOS transistor, the N well 46 for isolation by installation of an N type impurity is formed. And it has fixed spacing in the substrate front-face side in this N well 46, and is P+. The diffusion fields 47 and 48 are formed and they are these P+. A PMOS transistor is formed above the channel between the diffusion field 47 and 48 by the gate electrode 49 being arranged through gate dielectric film 44. Here, it is P+. The diffusion field 47 turns into the source / drain field, and it is P+. The diffusion field 48 turns into a drain / source field.
[0037] And N+ which becomes the source / drain field of an NMOS transistor in order to arrange both transistors in series P+ used as the diffusion field 43, and the source / drain field of a PMOS transistor The diffusion field 47 is connected by the aluminum (aluminum) wiring 50 through an interlayer insulation film 49. Moreover, N+ used as the drain / source field of an NMOS transistor P+ which the aluminum electrode 51 is connected to the diffusion field 42, and becomes the drain / source field of a PMOS transistor The aluminum electrode 52 is connected to the diffusion field 48.
[0038] Then, if the polish recon (polycrystalline silicon) of a bottom gate mold and the structure of TFT are considered, for example, as shown in drawing 6 , on a glass substrate 53, a fixed distance will be kept, the gate electrodes 54 and 55 will be formed, and the polish recon layer 57 will be formed through gate dielectric film 56 on it.
[0039] And the diffusion layer 60 used as the drain / source field of the diffusion layer 59 used as the source / drain field of the both sides of the diffusion layer 58 used as the drain / source field of an NMOS transistor, NMOS, and a PMOS transistor and a PMOS transistor is formed on the silicon oxide 56 of the side of the gate electrodes 54 and 55. The aluminum electrodes 62 and 63 are connected to diffusion layers 58 and 60 through an interlayer insulation film 61, respectively.
[0040] Since the well for isolation like [in the case of a single crystal silicon transistor] (46) does not exist in the case of poly-Si TFT so that clearly from contrast with the transistor structure of drawing 5 , and the transistor structure of drawing 6 , an NMOS transistor and a PMOS transistor are approached, continuation formation is attained, and as a result, the occupancy area of a circuit is very small and ends.
[0041] by the way, in the liquid crystal display using a common (VCOM) reversal drive, in the DA translation circuit which chooses the reference voltage of the level range of 0V-5V In order to secure the dynamic range of the reference voltage chosen when an MOS transistor is used as an analog switch as mentioned above If the threshold of Vthp and an NMOS transistor is set to Vthn for the threshold of a PMOS transistor, the low side of a select data signal must be 0 or less V-Vthp, and a high-level side must be 5 or more V+Vthn.
[0042] Thus, only the threshold Vthp of a PMOS transistor is low to the level range of reference voltage in the amplitude of a select data signal. And level range where only the threshold Vthn of an NMOS transistor is high (in the above-mentioned example) In the system configuration of drawing 1 since it is necessary to set up more than 0 V-Vthp - 5 V+Vthn with this operation gestalt The level shifter (level shift circuit) 124,134 has been arranged in the preceding paragraph of the DA translation circuit 125,135, and the configuration which attains the above-mentioned amplitude of a select data signal by the level shift in these level shifters 124,134 is taken.
[0043] According to this configuration, the reference voltage selection mold DA translation circuit of

small area can be realized, without setting up highly the supply voltage of the sampling & 1st latch circuit 122,132. However, when the amplitude of a select data signal from the first is what satisfies the above-mentioned conditions, even if it does not form a level shifter 124,134, it is clear that the dynamic range of the reference voltage chosen is securable.

[0044] Here, the concrete circuitry of the level shift circuit used as a level shifter 124,134 is explained.

[0045] Drawing 7 is the circuit diagram showing the 1st example of a level shift circuit. The level shift circuit concerning this 1st example is considering the CMOS latch cel 70 which comes to connect with juxtaposition CMOS inverter 71 with which each gate and drain consist of the NMOS transistor Qn11 and the PMOS transistor Qp11 which were connected in common, respectively, and CMOS inverter 72 of each other between a power source VDD and a gland with which each gate and drain consist of the NMOS transistor Qn12 and the PMOS transistor Qp12 which were connected in common, respectively as the basic configuration.

[0046] In this CMOS latch cel 70 The input edge of CMOS inverter 71 (namely, common gate node of MOS transistors Qn11 and Qp11), The outgoing end (namely, drain common node of MOS transistors Qn12 and Qp12) of CMOS inverter 72 is connected. Furthermore, the input edge (namely, common gate node of MOS transistors Qn12 and Qp12) of CMOS inverter 72 and the outgoing end (namely, drain common node of MOS transistors Qn11 and Qp11) of CMOS inverter 71 are connected.

[0047] Moreover, a resistance element R11 is connected between the input edge of CMOS inverter 71, and the 1st circuit input terminal 73, and the resistance element R12 is connected, respectively between the input edge of CMOS inverter 72, and the 2nd circuit input terminal 74. Furthermore, a resistance element R13 is connected between the input edge of CMOS inverter 71, and a power source VDD, and the resistance element R14 is connected between the input edge of CMOS inverter 72, and the power source VDD, respectively. Moreover, the inverter 78 is connected [between node **s and the 1st circuit output terminals 75 which are the common node of resistance elements R12 and R14], respectively between node **s and the 2nd circuit output terminals 76 whose inverter 77 is the common node of resistance elements R11 and R12.

[0048] In the level shift circuit concerning the 1st example of the above-mentioned configuration, the signal in 1 of the about [3V] amplitude **** shall be inputted into the 1st circuit input terminal 73, and the signal in 2 of reversal of an input signal in 1 shall be inputted into the 2nd circuit input terminal 74.

[0049] If it explains here using the timing of drawing 8 taking the case of circuit actuation in case an input signal in 1 is logic "1" (=****) and an input signal in 2 is logic "0" (=0V), it will set in the CMOS latch cel 70. Since a current will flow in the path of a power-source VDD-> resistance element R14 -> node **->NMOS transistor Qn11 -> gland since the NMOS transistor Qn11 will be in an ON state, and the PMOS transistor Qp12 will be in an ON state at coincidence, a power-source VDD->PMOS transistor -- a current flows in the path of the Qp12 -> node **-> resistance element R11 -> 2nd circuit input terminal 73.

[0050] At this time, a voltage drop arises in resistance elements R11 and R14, and the potential of node ** and ** rises by that voltage drop. That is, the potential of node ** and ** carries out DC shift. Here, for the node **, rather than node **, since the shift amount is large, by node ** and **, a bigger amplitude difference than the amplitude difference of input signals in1 and in2 will be acquired.

[0051] Moreover, resistance elements R13 and R14 make the operation which clarifies the operating point of CMOS inverters 71 and 72 more by carrying out bias of node ** and the **. And it is reversed with an inverter 77 and the potential of node ** is drawn from the 1st circuit output terminal 75 as an output signal out of the amplitude of VDD, it is reversed with an inverter 78 and the potential of node ** is drawn from the 2nd circuit output terminal 76 as a reversal signal xout of an output signal out.

[0052] The level shift of the input signals in1 and in2 which are 3V will be carried out to the output signal out of the amplitude of supply voltage VDD, and xout by the circuit actuation mentioned above, and the amplitude **** will be drawn. Moreover, when an input signal in 1 is logic "0" and an input signal in 2 is logic "0", level shift actuation will be performed by actuation completely

contrary to the actuation mentioned above.
[0053] Thus, the two input sections of the CMOS latch cel 70, i.e., each input edge of CMOS inverters 71 and 72 and two sources of an input signal, Namely, resistance elements R11 and R12 are connected between two circuit input terminals 73 and 74 into which input signals in1 and in2 are inputted. Since sufficient electrical potential difference for making each transistor which constitutes the CMOS latch cel 70 by carrying out DC shift of the input signals in1 and in2, and having made it give the two input sections of the CMOS latch cel 70 turn on can be obtained, Even if it is a device with a large threshold Vth, for example, the circuit using TFT, the stable level shift actuation is realizable at high speed.
[0054] And while only accumulating that a resistance element may be added to the basic circuit of the CMOS latch cel 70 and being able to realize in small area, since level shift actuation can be ensured even if it lowers supply voltage VDD, low-power-ization can be attained. Furthermore, since the operating point of CMOS inverters 71 and 72 can be clarified more by connecting resistance elements R13 and R14 also between the two input sections of the CMOS latch cel 70, and power sources VDD, and having been made to carry out bias of node ** and the **, the level shift actuation stabilized more is realizable.
[0055] In addition, as an input signal in 2 although [in the level shift circuit concerning the 1st example] the reversal signal of an input signal in 1 is considered as an input, since it is the translation which just distinguishes the logic of an input signal in 1, it is not necessary to be necessarily a reversal signal, and it is also possible to use the direct current voltage of the arbitration of within the limits from 0V to supply voltage VDD as reference voltage Vref of the distinction. The timing chart at the time of inputting reference voltage Vref (0 <=Vref<=VDD) into drawing 9 as an input signal in 2 is shown.
[0056] Moreover, although it has composition which derives two output signals out of reversal by being noninverting, and xout in the example of a circuit of drawing 7 , you may be the configuration which derives only one of output signals. In this case, one side of the two inverters 77 and 78 becomes unnecessary.
[0057] Drawing 10 is the circuit diagram showing the modification of the level shift circuit concerning the 1st example, and attaches and shows the same sign among drawing to drawing 7 and an equivalent part. In the level shift circuit concerning this modification, each gate has composition using the PMOS transistors Qp13 and Qp14 connected to the gland as resistance elements R13 and R14 as resistance elements R11 and R12 of drawing 7 using the NMOS transistors Qn13 and Qn14 by which each gate was connected to the power source VDD.
[0058] Thus, when resistance elements R11-R14 are realized with a transistor, actuation of the circuit is also the same as the case of the circuit of drawing 7 . Moreover, it is the same as drawing 8 and drawing 9 also about the example of timing. In addition, although resistance elements R11 and R12 are realized by NMOS and this modification has realized resistance elements R13 and R14 by PMOS, as long as it arranges a transistor so that it may become a form equivalent to these resistance elements, whichever is sufficient as the polarity of each transistor.
[0059] Drawing 11 is the circuit diagram showing other modifications of the level shift circuit concerning the 1st example, and attaches and shows the same sign among drawing to drawing 10 and an equivalent part. In the level shift circuit concerning this modification, it has composition which switches the NMOS transistors Qn13 and Qn14 and the PMOS transistors Qp13 and Qp14 with the control signal CNTL in the circuit of drawing 10 . That is, while the control signal CNTL of active"H" inputted into the control terminal 79 from the control circuit which is not illustrated is impressed to each gate of the NMOS transistors Qn13 and Qn14, it is reversed with an inverter 79 and is impressed by each gate of the PMOS transistors Qp13 and Qp14.
[0060] Thus, by taking the configuration which switches each transistors Qn13, Qn14, Qp13, and Qp14 of the CMOS latch cel 70 with the control signal CNTL, by the way, it is accepted and activates, and when [which is the need for a level shift about this level shift circuit] there is no need for a level shift, data in 1, i.e., an input signal, and the so-called latch combination type holding 1n of logic states of 2 of level shift circuit can be realized.
[0061] In addition, when resistance elements R11-R14 are realized with a transistor, although [this example] switching control of these transistors is carried out, even if it is made to carry out

switching control of these switches using the switch which has the resistance of finite as resistance elements R11-R14, the same operation effectiveness can be acquired.

[0062] Drawing 12 is the circuit diagram showing the modification of further others of the level shift circuit concerning the 1st example, and attaches and shows the same sign among drawing to drawing 11 and an equivalent part. In the level shift circuit concerning this modification, it has composition which added the reset circuit 81 for deciding the initial value of the CMOS latch cel 70 to be the circuit of drawing 11 further. This reset circuit 81 is constituted by the PMOS transistor Qp15 connected between a power source VDD and node **, and the gate of this PMOS transistor Qp15 is connected to the reset terminal 82.

[0063] And reset-signal Reset is given to the reset terminal 82. Here, as reset-signal Reset, as shown in the timing chart of drawing 13 , the signal which starts to the timing which was late for supply voltage VDD is used. This reset-signal Reset can be simply generated by integrating the RC integrating circuit 83 with supply voltage VDD, as shown in drawing 14 .

[0064] Thus, the initial value in the CMOS latch cel 70 at the time of power-source starting can be determined by adding a reset circuit 81 to the circuit of drawing 11 further, and giving reset-signal Reset which starts to the timing which was late for supply voltage VDD to this reset circuit 81. By this reset action, in this example, the potential of node ** serves as "H" level by the initial state at the time of power-source starting, and an output signal out serves as "L" level so that clearly from the timing chart of drawing 13 .

[0065] Drawing 15 is the circuit diagram showing the 2nd example of a level shift circuit. The level shift circuit concerning this 2nd example has the composition that CMOS inverter 85 with which each gate and drain consist of the NMOS transistor Qn21 and the PMOS transistor Qp21 which were connected in common, and CMOS inverter 86 with which each gate and drain consist of the NMOS transistor Qn22 and the PMOS transistor Qp22 which were connected in common made the basic circuit the CMOS latch cel 84 which it comes to connect each other between a power source VDD and a gland with juxtaposition.

[0066] In this CMOS latch cel 84 The input edge of CMOS inverter 85 (namely, common gate node of MOS transistors Qn21 and Qp21),

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CLAIMS

[Claim(s)]
[Claim 1] n polar analog switches corresponding to the logic of each bit of a n bits (n be two or more integers) data signal be mutually connect to a serial, and it become, and be 2n. 2n connected between each of the reference voltage line of a book, and an output line, respectively Digital to analog circuit characterize by have the gradation selection unit of an individual.
[Claim 2] Said n analog switches are digital-to-analog circuits according to claim 1 respectively characterized by consisting of one MOS transistor of the conductivity type corresponding to the logic of each bit of said data signal.
[Claim 3] The amplitude of said data signal is a digital-to-analog circuit according to claim 2 characterized by being more than the level range where only the threshold of an N-channel metal oxide semiconductor transistor is high low [the threshold of a P channel MOS transistor] to the level range of reference voltage.
[Claim 4] The 1st substrate with which the effective pixel field which consists of two or more pixels, and the drive circuit including a digital-to-analog circuit were formed, The 2nd substrate by which opposite arrangement was carried out with predetermined spacing to said 1st substrate, It is a liquid crystal display possessing the liquid crystal layer held between said 1st substrate and said 2nd substrate. Said digital-to-analog circuit It comes to connect n polar analog switches corresponding to the logic of each bit of a n bits (n is two or more integers) data signal with a serial mutually. And 2n 2n connected between the reference voltage line of a book, and the column line of a picture element part, respectively Liquid crystal display characterized by having the gradation selection unit of an individual.
[Claim 5] Each pixel of said effective pixel field is a liquid crystal display according to claim 4 characterized by driving by the common reversal drive which reverses the common electrical potential difference impressed common to the counterelectrode of a liquid crystal cell for every 1 level period.
[Claim 6] The shift register which outputs a sampling pulse sequentially from each transfer stage by said drive circuit's consisting of two or more transfer stages, answering a start signal, and performing a shift action, The 1st latch circuit which carries out a sequential sampling and latches a data signal from each transfer stage of said shift register synchronizing with the sampling pulse outputted, The signal sampled by said 1st latch circuit is latched for every 1 level period corresponding to each column line. The 2nd latch circuit which supplies the latched signal to said digital-to-analog circuit is provided. Said shift register While having the 1st level shift circuit which carries out the level shift of said start signal, and is supplied to the transfer stage of the first rank, and the 2nd level shift circuit which carries out the level shift of the clock signal, and is supplied to the transfer stage of each stage The said 1st and 2nd level shift circuit considers a CMOS latch cel as a basic configuration. It has the resistance element inserted, respectively between the two input sections of said CMOS latch cel, and two sources of an input signal. Said 1st latch circuit The 1st switch which considered the CMOS latch cel as the basic configuration, and was connected, respectively between the two input sections of said CMOS latch cel, and two input signal lines, The 2nd switch connected between power-source Rhine the power-source side of said CMOS latch cel, It has the control means which carries out switching control of said the 1st switch and said 2nd switch complementary. Said 2nd latch circuit The 1st and 2nd switch which chooses the 1st and 2nd power source from which a CMOS latch cel is

considered as a basic configuration, it is prepared at least in one side by the side of the positive supply of said CMOS latch cel, and a negative supply, and supply voltage differs, respectively, The liquid crystal display according to claim 4 characterized by having the control means which carries out switching control of said 1st and 2nd switch according to each period of latch actuation of said CMOS latch cel, and output actuation.
[Claim 7] Said drive circuit between said 2nd latch circuit and said digital-to-analog circuits The level shift circuit which carries out the level shift of the signal latched by said 2nd latch circuit, and is supplied to said digital-to-analog circuit is provided. Said level shift The liquid crystal display according to claim 6 which considers a CMOS latch cel as a basic configuration, and is characterized by having the resistance element inserted, respectively between the two input sections of said CMOS latch cel, and two sources of an input signal.

[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the system configuration of the drive circuit one apparatus liquid crystal display concerning 1 operation gestalt of this invention.
[Drawing 2] It is the circuit diagram showing an example of the configuration of an effective pixel field.
[Drawing 3] It is the basic block diagram of a reference voltage selection mold DA translation circuit.
[Drawing 4] It is the circuit diagram showing the concrete circuitry of a reference voltage selection mold DA translation circuit.
[Drawing 5] It is the sectional view showing an example of the structure of a single crystal silicon transistor.
[Drawing 6] It is the sectional view showing an example of the structure of poly-Si TFT.
[Drawing 7] It is the circuit diagram showing the 1st example of a level shift circuit.
[Drawing 8] It is a timing chart for explaining circuit actuation of the level shift circuit concerning the 1st example.
[Drawing 9] It is a timing chart at the time of making direct current voltage into reference voltage.
[Drawing 10] It is the circuit diagram showing the modification of the level shift circuit concerning the 1st example.
[Drawing 11] It is the circuit diagram showing other modifications of the level shift circuit concerning the 1st example.
[Drawing 12] It is the circuit diagram showing the modification of further others of the level shift circuit concerning the 1st example.
[Drawing 13] It is a timing chart for explaining the circuit actuation at the time of adding a reset circuit.
[Drawing 14] It is the circuit diagram showing the example of a circuit which generates a reset signal.
[Drawing 15] It is the circuit diagram showing the 2nd example of a level shift circuit.
[Drawing 16] It is the circuit diagram showing the modification of the level shift circuit concerning the 2nd example.
[Drawing 17] It is the block diagram showing an example of the configuration of a level shift register.
[Drawing 18] It is the circuit diagram showing the 1st example of a sampling hold circuit.
[Drawing 19] It is a timing chart for explaining circuit actuation of the sampling hold circuit concerning the 1st example.
[Drawing 20] It is a timing chart at the time of making the reversal signal of an input signal in 1 into an input signal in 2.
[Drawing 21] It is the circuit diagram showing the modification of the sampling hold circuit concerning the 1st operation gestalt.
[Drawing 22] It is the circuit diagram showing the 2nd example of a sampling hold circuit.
[Drawing 23] It is the block diagram showing an example of the concrete configuration at the time of using the sampling hold circuit concerning each example as the sampling & 1st latch circuit.
[Drawing 24] It is the block diagram showing the configuration at the time of making the reversal

data of digital data into an input signal in 2.
[Drawing 25] It is the block diagram showing the modification of drawing 24 .
[Drawing 26] It is the circuit diagram showing the 1st example of a latch circuit.
[Drawing 27] It is a timing chart for explaining circuit actuation of the latch circuit concerning the 1st operation gestalt.
[Drawing 28] It is the timing chart which shows another example of timing of circuit actuation of the latch circuit concerning the 1st operation gestalt.
[Drawing 29] It is the circuit diagram showing the example of the latch circuit concerning the 1st operation gestalt.
[Drawing 30] It is the circuit diagram showing the 2nd example of a latch circuit.
[Drawing 31] It is the circuit diagram showing the 3rd example of a latch circuit.
[Drawing 32] It is the block diagram showing an example of the concrete configuration at the time of using the latch circuit concerning each operation gestalt as the 2nd latch circuit.
[Drawing 33] It is the block diagram showing the modification of drawing 32 .
[Drawing 34] It is the block diagram showing the system configuration of the conventional example.
[Drawing 35] It is the circuit diagram showing an example of a reference voltage selection mold DA translation circuit.
[Description of Notations]
11 -- 12 An effective pixel field, 13 -- The 1st and 2nd level drive system, 14 -- Vertical-drive system, 20 -- A pixel, 21 -- TFT (thin film transistor), 22 -- Liquid crystal cell, 23 -- Auxiliary capacity, 30-37 -- 70 A gradation selection unit, 84,100,150,170,190 -- CMOS latch cel, 71, 72, 85, 86, 101, 102, 151, 152, 171,172,191,192 -- CMOS inverter, 121,131 -- A level shift register, 122,132 -- The sampling & 1st latch circuit (sampling latch circuit), 123,133 -- The 2nd latch circuit (latch circuit), 124,134 -- Level shifter (level shift circuit), 125,135 -- A DA translation circuit, 301-303,311-313,321-323,331-333,341-343,351-353,361-363,371-373 -- An analog switch, Vref0-Vref7 -- Reference voltage

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[Translation done.]

* NOTICES *

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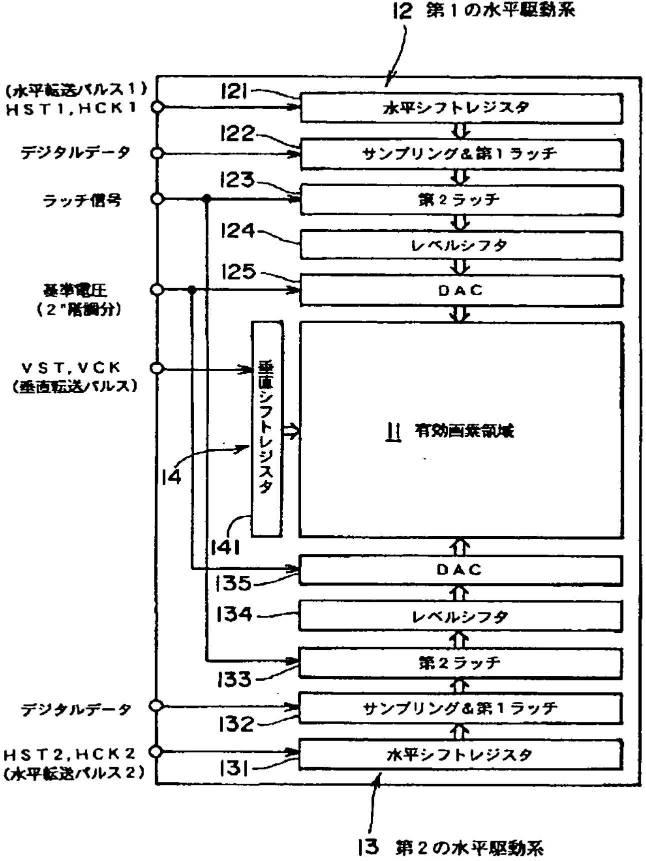
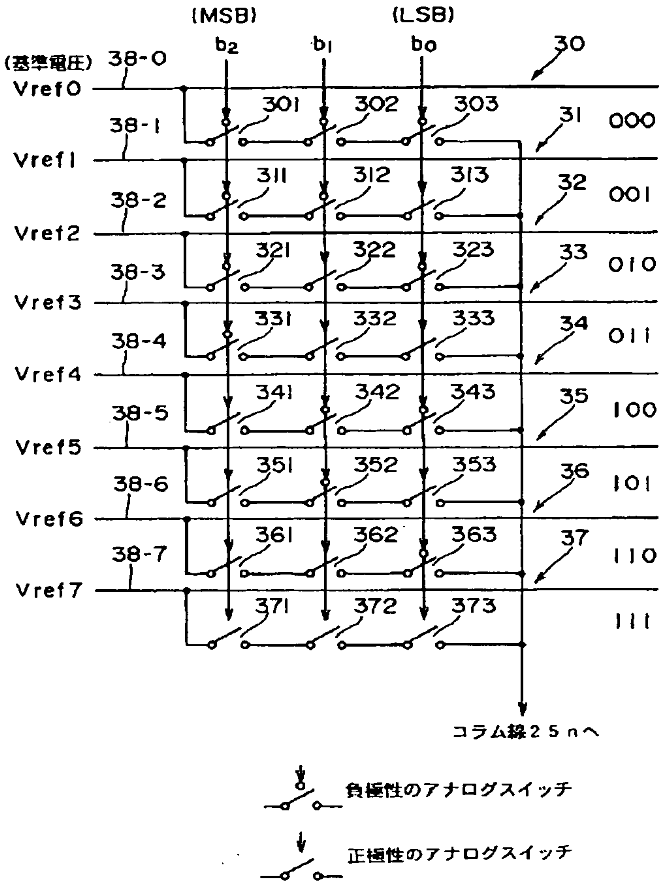
3.In the drawings, any words are not translated.

DRAWINGS

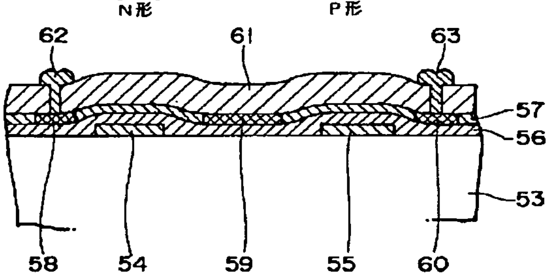
[Drawing 1]


12 第１の水平駆動系
(水平転送パルス１)
HST1,HCK1
デジタルデータ
ラッチ信号
基準電圧
(2ⁿ階調分)
VST,VCK
(垂直転送パルス)
14
141
デジタルデータ
HST2,HCK2
(水平転送パルス２)
121
水平シフトレジスタ
122
サンプリング＆第１ラッチ
123
第２ラッチ
124
レベルシフタ
125
DAC
垂直シフトレジスタ
11 有効画素領域
DAC
135
レベルシフタ
134
第２ラッチ
133
サンプリング＆第１ラッチ
132
水平シフトレジスタ
131
13 第２の水平駆動系

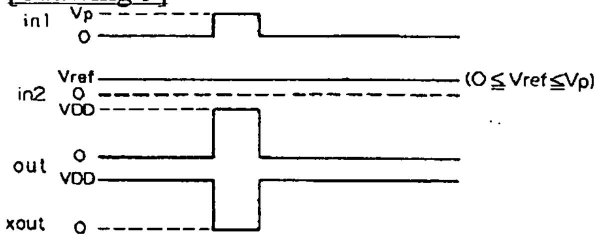
[Drawing 3]


(MSB)
(LSB)
b2
b1
b0
30
(基準電圧)
38-0
Vref0
301
302
303
31
000
38-1
Vref1
311
312
313
32
001
38-2
Vref2
321
322
323
33
010
38-3
Vref3
331
332
333
34
011
38-4
Vref4
341
342
343
35
100
38-5
Vref5
351
352
353
36
101
38-6
Vref6
361
362
363
37
110
38-7
Vref7
371
372
373
111
コラム線２５ｎへ
負極性のアナログスイッチ
正極性のアナログスイッチ

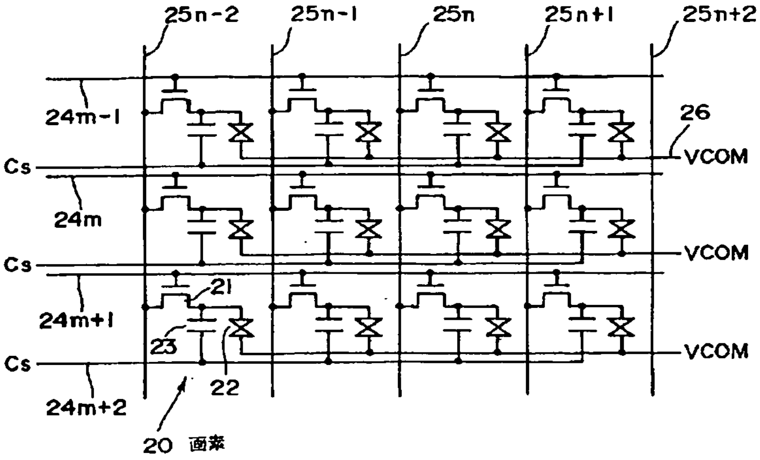
[Drawing 6]


N形
P形
62
61
63
57
56
53
58
54
59
55
60

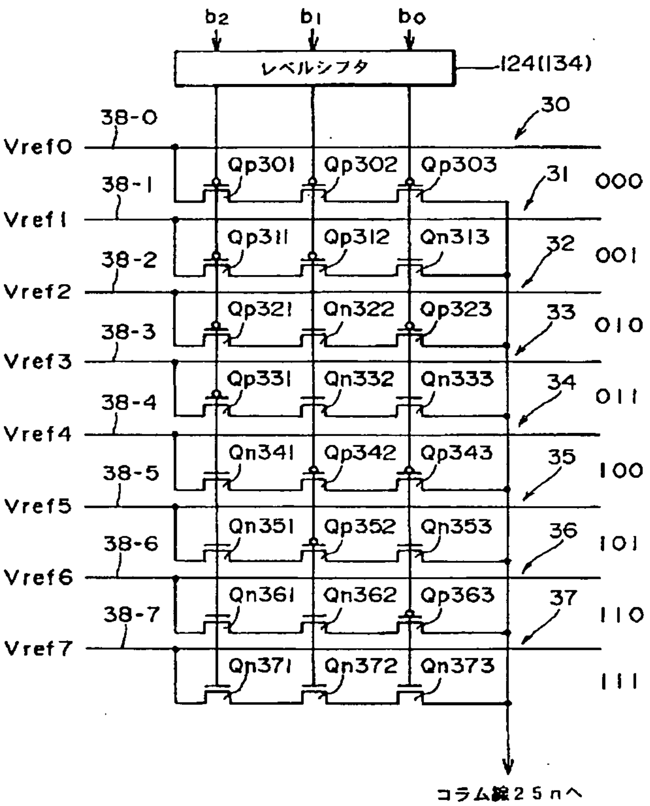
[Drawing 9]



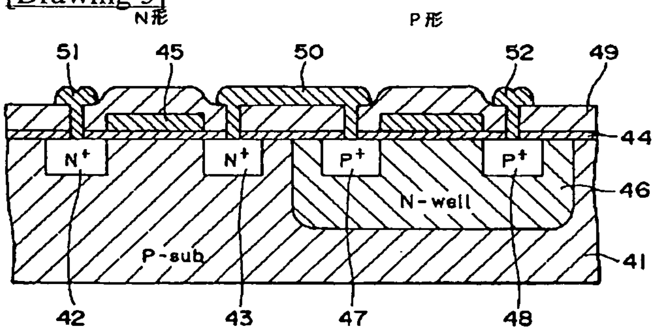
[Drawing 2]


25n-2
25n-1
25n
25n+1
25n+2
24m-1
26
VCOM
Cs
24m
VCOM
Cs
21
24m+1
23
22
Cs
VCOM
24m+2
22
20 画素

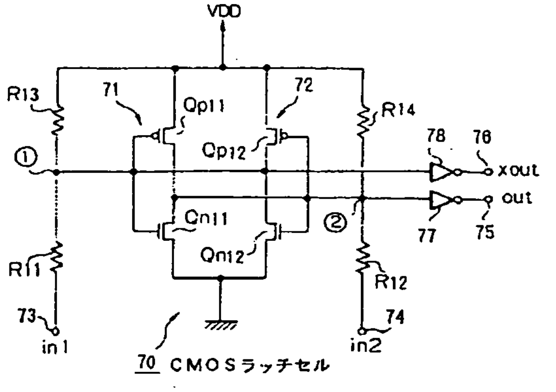
[Drawing 4]


(MSB)
b2
b1
(LSB)
b0
レベルシフタ
124(134)
30
38-0
Vref0
Qp301
Qp302
Qp303
31
000
38-1
Vref1
Qp311
Qp312
Qn313
32
001
38-2
Vref2
Qp321
Qn322
Qp323
33
010
38-3
Vref3
Qp331
Qn332
Qn333
34
011
38-4
Vref4
Qn341
Qp342
Qp343
35
100
38-5
Vref5
Qn351
Qp352
Qn353
36
101
38-6
Vref6
Qn361
Qn362
Qp363
37
110
38-7
Vref7
Qn371
Qn372
Qn373
111
コラム線25nへ

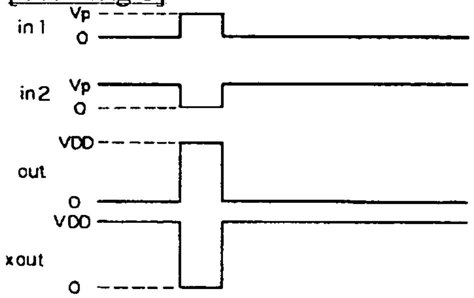
[Drawing 5]


N形
P形
51
45
50
52
49
44
N+
N+
P+
P+
N-well
46
P-sub
41
42
43
47
48

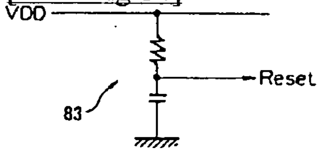
[Drawing 7]


VDD
R13
71
Qp11
72
R14
①
Qp12
78
76
xout
out
Qn11
②
77
75
Qn12
R11
R12
73
74
in1
in2
70 CMOSラッチセル

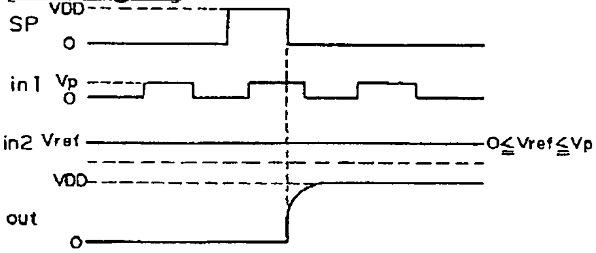
[Drawing 8]



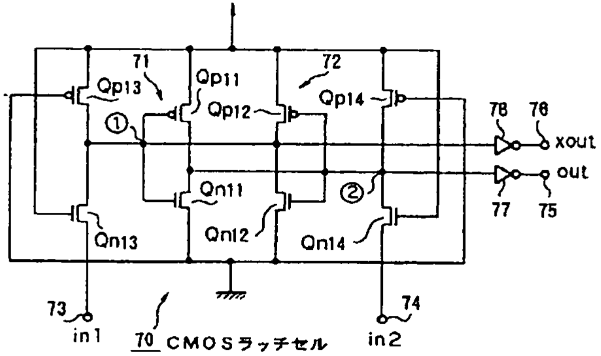
[Drawing 14]


VDD
Reset
83

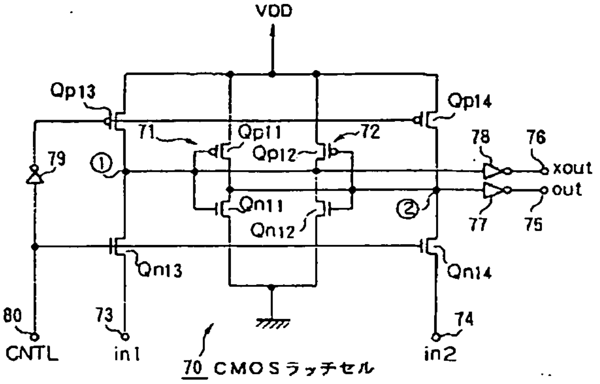
[Drawing 19]



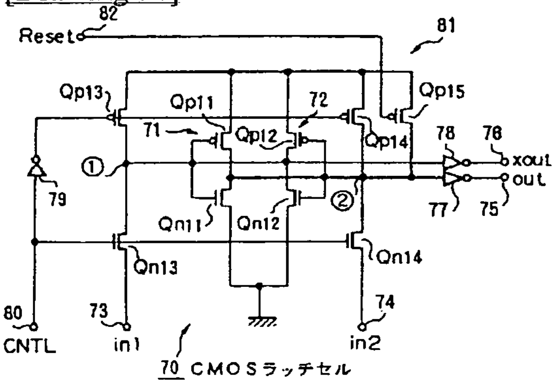
[Drawing 10]


VDD
71
Qp11
72
Qp13
Qp12
Qp14
①
78
76
xout
out
Qn11
②
77
75
Qn13
Qn12
Qn14
73
74
in1
in2
70 CMOSラッチセル

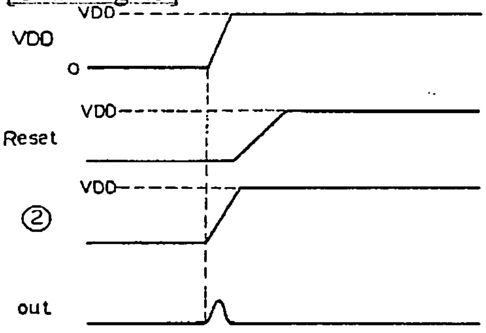
[Drawing 11]


VDD
Qp13
Qp14
71
Qp11
Qp12
72
78
76
xout
out
79
①
Qn11
Qn12
②
77
75
Qn13
Qn14
80
CNTL
73
in1
74
in2
70 CMOSラッチセル

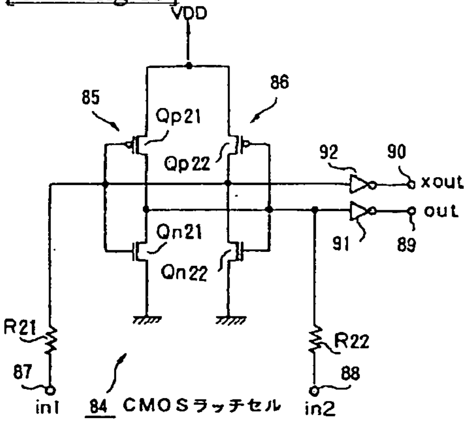
[Drawing 12]


82
Reset
81
Qp13
Qp11
72
Qp15
71
Qp12
Qp14
78
76
xout
out
①
79
Qn11
Qn12
②
77
75
Qn13
Qn14
80
CNTL
73
in1
74
in2
70 CMOSラッチセル

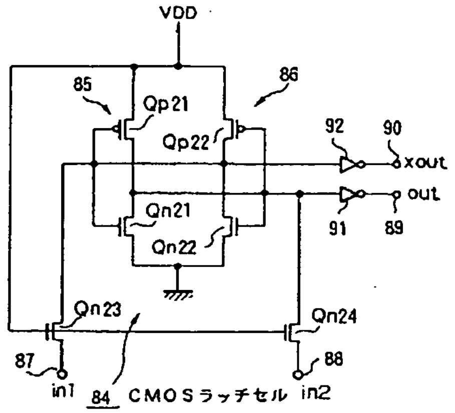
[Drawing 13]



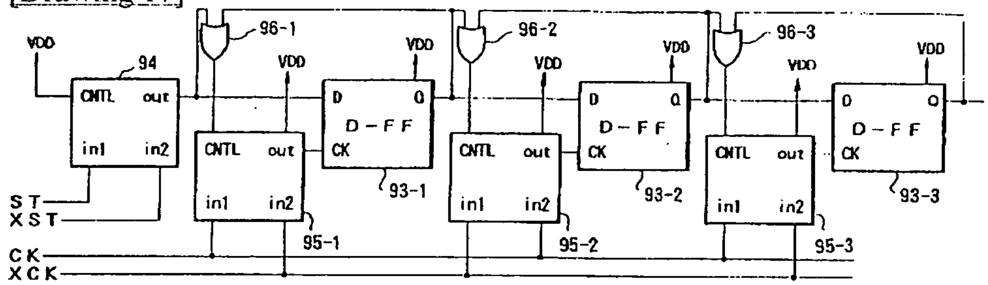
[Drawing 15]


VDD
85
86
Qp21
Qp22
92
90
xout
out
Qn21
Qn22
91
89
R21
R22
87
88
in1
84 CMOSラッチセル
in2

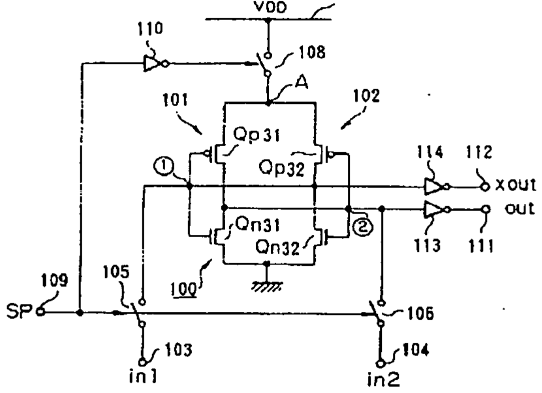
[Drawing 16]


VDD
85
86
Qp21
Qp22
92
90
xout
out
Qn21
Qn22
91
89
Qn23
Qn24
87
88
in1
84
CMOSラッチセル
in2

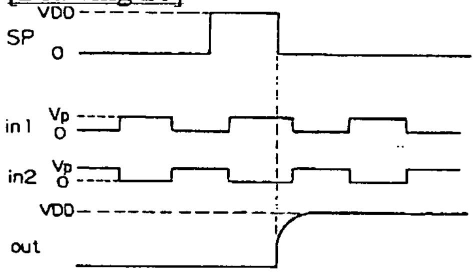
[Drawing 17]


VDD
94
CNTL
out
in1
in2
96-1
96-2
96-3
D
Q
D－FF
CK
93-1
93-2
93-3
95-1
95-2
95-3
ST
XST
CK
XCK

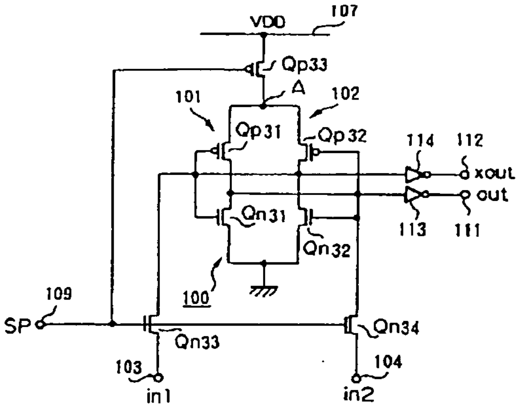
[Drawing 18]


VDD
107
110
108
A
101
102
Qp31
Qp32
①
114
112
xout
out
Qn31
Qn32
②
113
111
100
109
SP
105
106
103
104
in1
in2

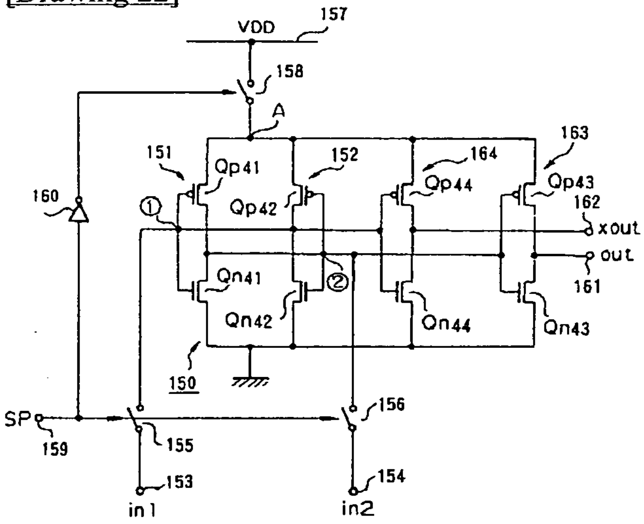
[Drawing 20]



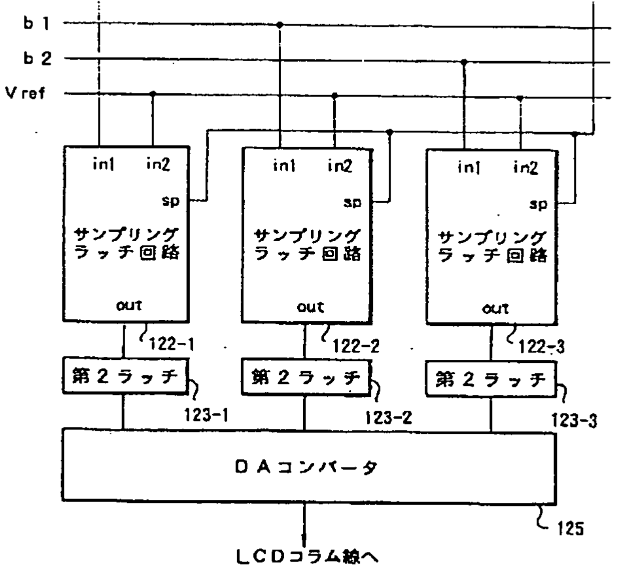
[Drawing 21]


VDD
107
Qp33
A
101
102
Qp31
Qp32
114
112
xout
out
Qn31
Qn32
113
111
109
100
SP
Qn33
Qn34
103
104
in1
in2

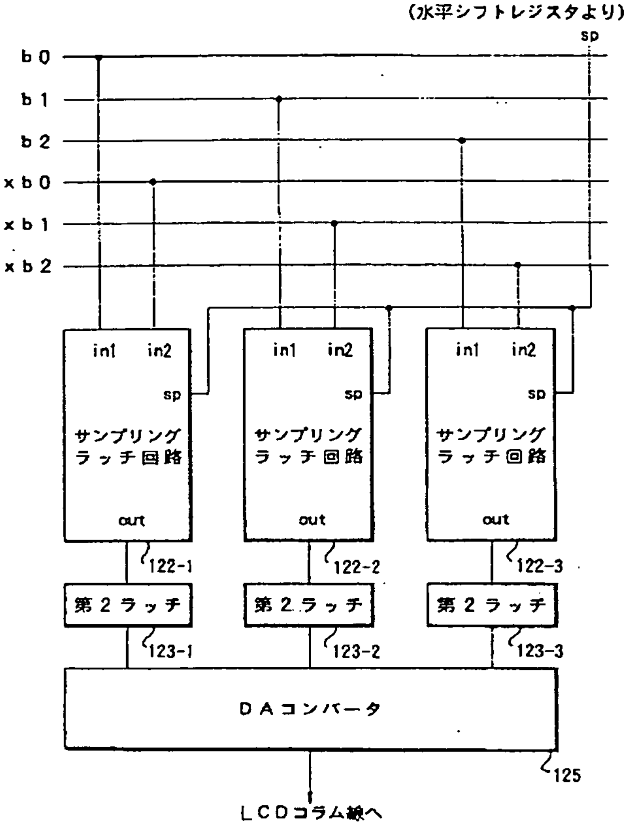
[Drawing 22]


VDD
157
158
A
151
152
164
163
Qp41
Qp44
Qp43
160
①
Qp42
162
xout
out
161
Qn41
②
Qn42
Qn44
Qn43
150
SP
159
155
156
153
154
in1
in2

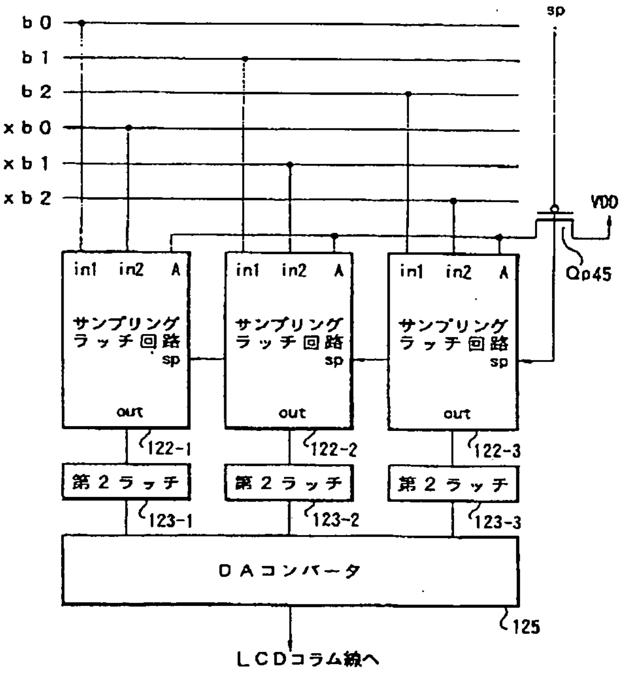
[Drawing 23]


(水平シフトレジスタより)
sp
b 0
b 1
b 2
V ref
in1
in2
sp
サンプリング
ラッチ回路
out
122-1
122-2
122-3
第2ラッチ
123-1
123-2
123-3
DAコンバータ
125
LCDコラム線へ

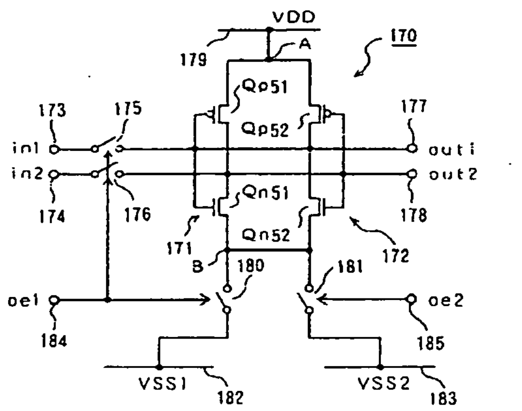
[Drawing 24]


(水平シフトレジスタより)
sp
b 0
b 1
b 2
x b 0
x b 1
x b 2
in1
in2
sp
サンプリング
ラッチ回路
out
122-1
122-2
122-3
第2ラッチ
123-1
123-2
123-3
DAコンバータ
125
LCDコラム線へ

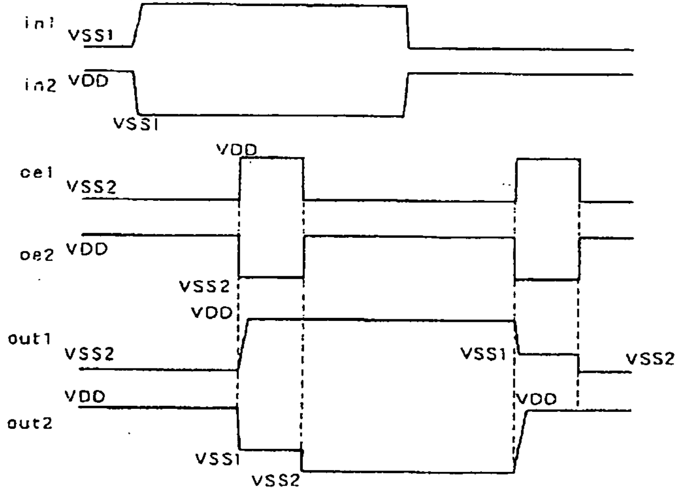
[Drawing 25]


(水平シフトレジスタより)
sp
b 0
b 1
b 2
x b 0
x b 1
x b 2
VDD
Qp45
in1
in2
A
サンプリング
ラッチ回路
sp
out
122-1
122-2
122-3
第2ラッチ
123-1
123-2
123-3
DAコンバータ
125
LCDコラム線へ

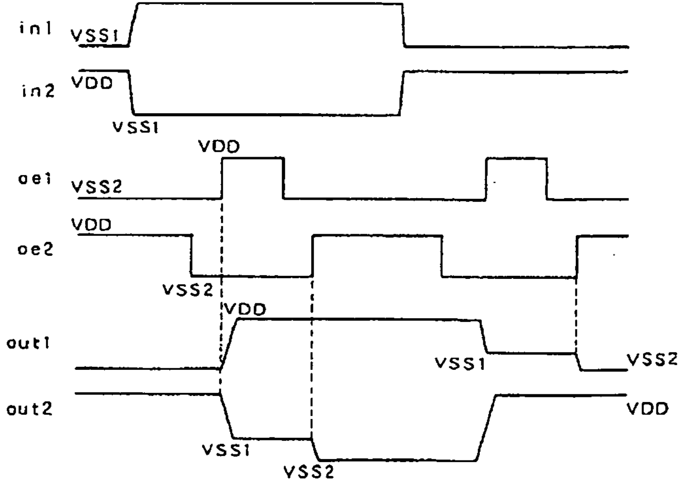
[Drawing 26]


VDD
170
179
A
Qp51
Qp52
173
175
177
in1
in2
out1
out2
174
176
178
Qn51
Qn52
171
172
B
180
181
oe1
oe2
184
185
VSS1
182
VSS2
183

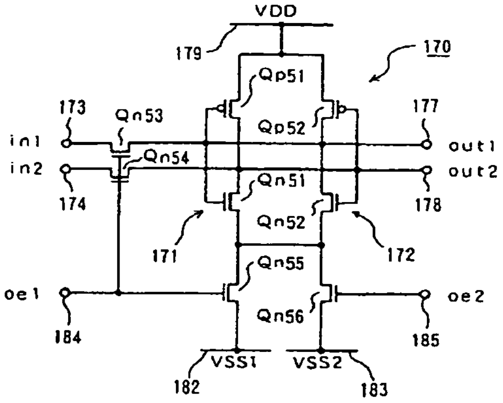
[Drawing 27]



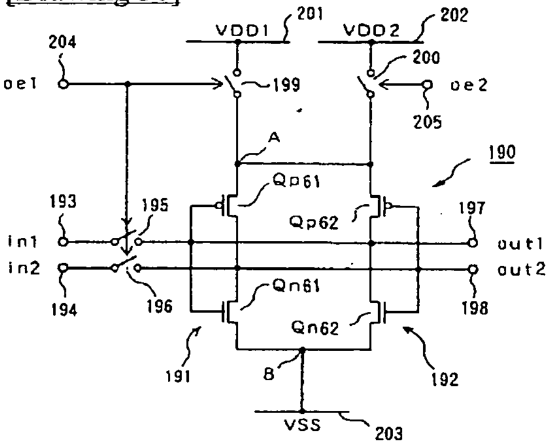
[Drawing 28]



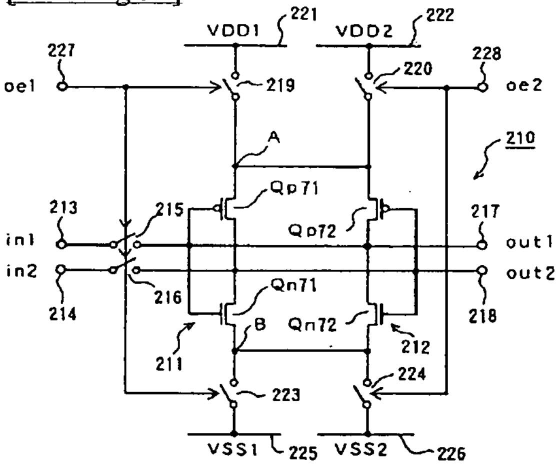
[Drawing 29]


VDD
179
170
Qp51
Qp52
173
Qn53
177
in1
out1
in2
Qn54
out2
174
Qn51
178
Qn52
171
172
Qn55
oe1
oe2
Qn56
184
185
VSS1
VSS2
182
183

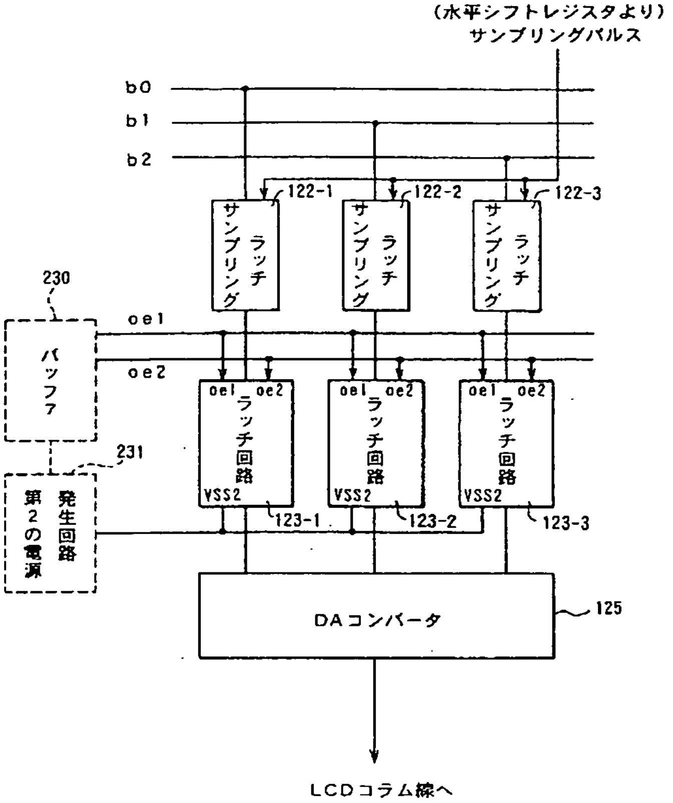
[Drawing 30]


VDD1
201
VDD2
202
204
200
oe1
199
oe2
205
A
190
Qp61
193
195
Qp62
197
in1
out1
in2
out2
194
196
Qn61
198
Qn62
191
B
192
VSS
203

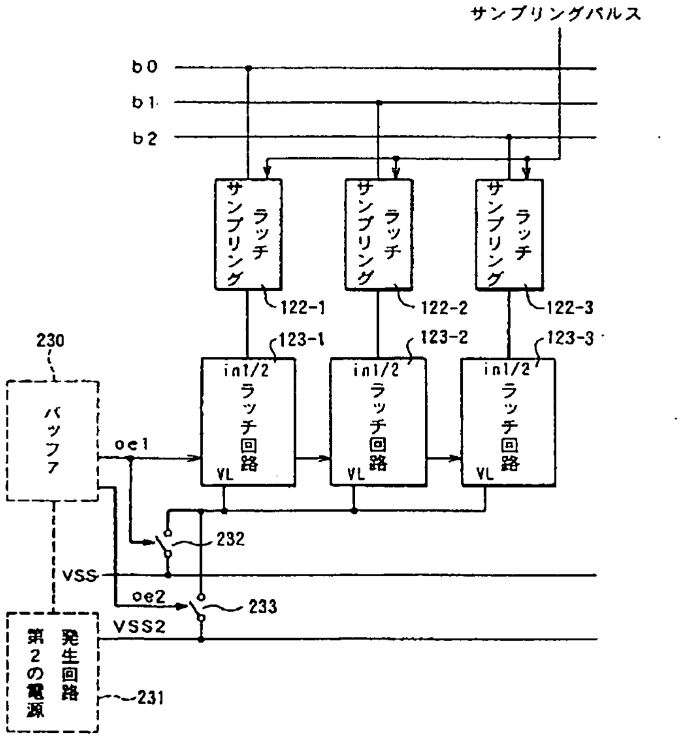
[Drawing 31]


VDD1
221
VDD2
222
227
220
228
oe1
219
oe2
A
210
Qp71
213
215
217
Qp72
in1
out1
in2
out2
216
214
Qn71
218
B
Qn72
211
212
224
223
VSS1
225
VSS2
226

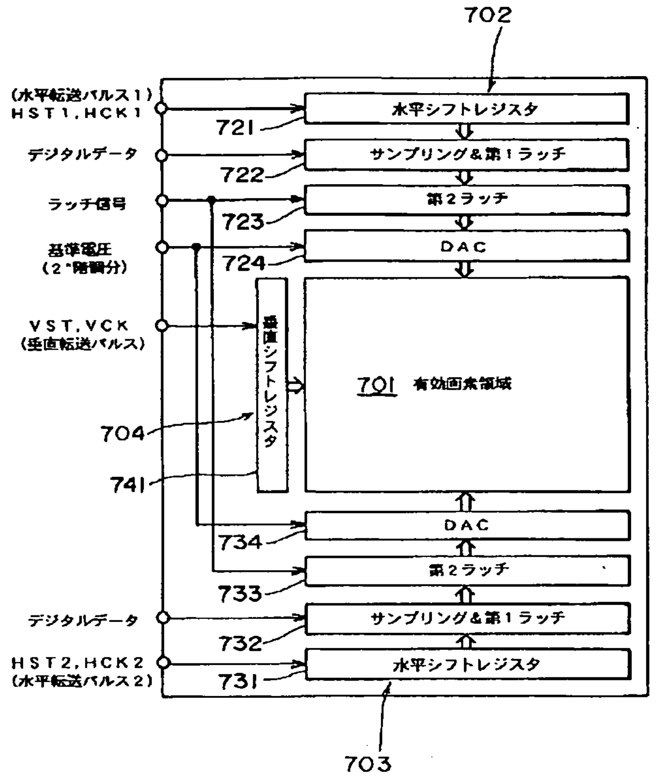
[Drawing 32]


（水平シフトレジスタより）
サンプリングパルス
b0
b1
b2
122-1
122-2
122-3
サンプリングラッチ
サンプリングラッチ
サンプリングラッチ
230
バッファ
oe1
oe2
oe1 oe2
ラッチ回路
VSS2
ラッチ回路
VSS2
ラッチ回路
VSS2
231
第2の電源発生回路
123-1
123-2
123-3
DAコンバータ
125
LCDコラム線へ

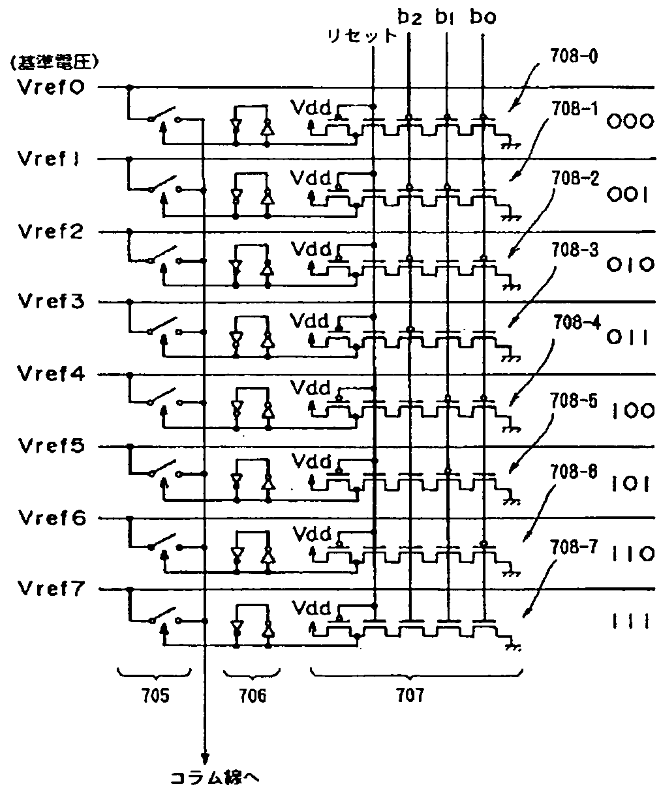
[Drawing 33]


（水平シフトレジスタより）
サンプリングパルス
b0
b1
b2
サンプリングラッチ
サンプリングラッチ
サンプリングラッチ
122-1
122-2
122-3
230
123-1
123-2
123-3
in1/2
ラッチ回路
VL
in1/2
ラッチ回路
VL
in1/2
ラッチ回路
VL
バッファ
oe1
232
VSS
oe2
233
VSS2
第2の電源発生回路
231

[Drawing 34]


702
(水平転送パルス1)
HST1, HCK1
水平シフトレジスタ
721
デジタルデータ
サンプリング&第1ラッチ
722
ラッチ信号
第2ラッチ
723
基準電圧
(2ⁿ階調分)
DAC
724
VST, VCK
(垂直転送パルス)
垂直シフトレジスタ
701 有効画素領域
704
741
DAC
734
第2ラッチ
733
デジタルデータ
サンプリング&第1ラッチ
732
HST2, HCK2
(水平転送パルス2)
水平シフトレジスタ
731
703

[Drawing 35]


(MSB) (LSB)
b2 b1 b0
リセット
(基準電圧)
Vref0
Vref1
Vref2
Vref3
Vref4
Vref5
Vref6
Vref7
Vdd
708-0
708-1
708-2
708-3
708-4
708-5
708-6
708-7
000
001
010
011
100
101
110
111
705
706
707
コラム線へ

[Translation done.]